REMARKS

Claims 1-22 have been rejected under 35 U.S.C. 102(e) as being anticipated by Whetsel (U.S. patent number 6,408,413).

Claim 1 has been amended to incorporate the limitations of Claim 20 (and Claim 20 has been canceled). Thus, Claim 1 as amended recites "wherein each of the test modules includes circuitry configured to route addresses received on the dedicated test bus to a corresponding one of the RAM blocks, whereby the corresponding one of the RAM blocks is accessed in response to the routed addresses".

Whetsel teaches "an architecture which permits plural TAPs to be selectively accessed and controlled from a single 1149.1 TAP interface". (Whetsel, Col. x, lines y.) The IEEE 1149.1 TAP interface uses a serial protocol, which does not include addresses for accessing RAM blocks. (See, e.g., Whetsel, Fig. 2.)

The Examiner's rejection indicates that test access ports TAP2-TAP4 correspond with a plurality of test modules as recited by Claim 1. Test access ports TAP2-TAP4 are coupled to megamodules MM1-MM3, respectively. (Whetsel, Fig. 2.) However, Whetsel fails to teach that each of the test access ports TAP2-TAP4 includes circuitry configured to receive "addresses … on the dedicated test bus" as recited by Claim 1. Indeed, the IEEE 1149.1 TAP interface implemented by Whetsel does not seem to require that test access ports TAP2-TAP4 receive any addresses. (Whetsel, Fig. 2.)

Moreover, even if Whetsel did teach that test access ports TAP2-TAP4 receive addresses, Whetsel would still fail to teach that such addresses should be routed from the test access ports TAP2-TAP4 'to a corresponding one of the RAM

blocks' as recited by Claim 1. Whetsel would further fail to teach that "the corresponding one of the RAM blocks is accessed in response to the routed addresses" as recited by Claim 1.

For these reasons, Claim 1 as amended is not anticipated by Whetsel. Claims 2-10 and 21-22, which depend from Claim 1, are not anticipated by Whetsel for at least the same reasons as Claim 1.

In addition, the Applicant does not believe that Whetsel teaches: "a switching structure" as recited by Claim 2; "a JTAG controller configured to control the switching structure" as recited by Claim 3; "dual-port and two-port RAM blocks" as recited by Claim 4; "a first set of lines for transmitting address and data signals to the test modules" and "a third set of one or more lines for transmitting a signal for latching the command signals" as recited by Claim 5; "a fourth set of lines for transmitting byte-enable signals to the test modules" as recited by Claim 6; "each of the test modules comprises a register for storing a unique address" as recited by Claim 8; or "wherein each of the RAM blocks has a capacity of 32 Kb or less" as recited by Claim 10. It is the Examiner's burden to indicate where Whetsel teaches these recited elements.

Claim 11, which has been amended to recite "the RAM blocks are accessed in response to addresses broadcast on the dedicated test bus", is not anticipated by Whetsel for reasons similar to Claim 11. Claims 12-19, which depend from Claim 11, not anticipated by Whetsel for reasons similar to Claim 11.

In addition, the Applicant does not believe that Whetsel teaches: "storing a unique address in each of the test modules" as recited by Claim 13; "coupling the pads to

the system circuitry during normal operation of the chip; and coupling the pads to the test bus during the test mode" as recited by Claim 14; "controlling the coupling of the pads using a JTAG controller" as recited by Claim 15; "writing test data values to the RAM blocks by broadcasting the test data values to all of the RAM blocks on the test bus; and then reading test data values from the RAM blocks by individually accessing the RAM blocks on the test bus" as recited by Claim 16; "writing test data values to RAM blocks having one write port and to the first write port of RAM blocks having more than one write port; and then writing test data values to the second write port of RAM blocks having more than one write port" as recited by Claim 17; "operating the test bus in response to a first clock signal during the test mode; and operating the RAM blocks in response to a second clock signal during the test mode, wherein the first clock signal and the second clock signal are independent signals" as recited by Claim 18; and "adjusting edges of the first clock signal relative to edges of the second clock signal" as recited by Claim 19. If the Examiner believes that these steps are taught by Whetsel, it is the Examiner's burden to show where Whetsel provides these teachings.

Claims 1-3 and 5-22 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Kraus et al. (U.S. Patent 6,587,979) and Cowles (U.S. Patent 6,212,114).

The Applicant renews the previous arguments to this rejection.

In addition, Kraus et al. fail to teach that "each of the test modules includes circuitry configured to route addresses received on the dedicated test bus to a

corresponding one of the RAM blocks, whereby the corresponding one of the RAM blocks is accessed in response to the routed addresses" as recited by amended Claim 1. Rather, Kraus et al. teach that addresses for each RAM 12 are generated locally in a corresponding core wrapper 24 using a pattern generator 50. (See, Kraus et al., Col. 7, lines 64-65; Col. 12, lines 11-14; Figs. 5 and 6.) Consequently, Kraus et al. teach away from the test module circuitry and dedicated test bus as recited by claim 1. Cowles does not remedy this deficiency of Kraus et al. For this additional reason, claim 1 is allowable over Kraus et al. and Cowles.

Claims 2-10 and 21-22, which depend from claim 1, are allowable over Kraus et al. and Cowles for at least the same reasons as claim 1.

In addition, Claim 11, which has been amended to recite "the RAM blocks are accessed in response to addresses broadcast on the dedicated test bus", is additionally allowable over Kraus et al. in view of Cowles for reasons similar to claim 1. Claims 12-19, which depend from claim 11, are allowable over Kraus et al. and Cowles for at least the same reasons as claim 11.

Claim 4 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Kraus et al., Cowles and Nadeau-Dostie et al. (U.S. Patent 5,812,469).

Claim 4, which depends from Claim 1 is allowable over Kraus et al. in view of Cowles for at least the same reasons as Claim 1. Nadeau-Dostie et al., which appears to be cited to introduce dual-port memory testing, does not remedy the above-described deficiencies of Krause et al. and Cowles.

Thus, Claim 4 is allowable over Krause et al. in view of Cowles and Nadeau-Dostie et al.

Claims 1-3 and 5-9 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Kraus et al., Cowles and Jamal (U.S. Patent 5,568,437).

As described above, Claim 1 is allowable over Kraus et al. in view of Cowles. Because Jamal does not teach or suggest a dedicated test bus as recited by Claim 1 (see, Applicant's Response to the First Office Action), Jamal fails to remedy the above-described deficiencies of Krause et al. and Cowles. Thus, Claim 1 is allowable over Krause et al. in view of Cowles and Jamal. Claims 2-3 and 5-9, which depend from Claim 1, are allowable over Kraus et al. in view of Cowles and Jamal for at least the same reasons as Claim 1.

Claims 10-18 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Kraus et al., Cowles, Jamal and Grider et al. (U.S. Patent 5,515,540).

As described above, Claim 1 is allowable over Kraus et al. in view of Cowles and Jamal. Grider et al., is cited for teaching memory blocks with a capacity of 32 Kb or less, does not remedy the above-described deficiencies of Krause et al., Cowles and Jamal. For this reason, Claim 1 is allowable over Krause et al. in view of Cowles, Jamal and Grider et al. Claim 10, which depends from Claim 1, is allowable over Kraus et al. in view of Cowles, Jamal and Grider et al. for at least the same reasons as Claim 1.

As described above, Claim 11 is allowable over Kraus et al. in view of Cowles. Jamal and Grider et al. do not remedy the above-described deficiencies of Krause et al. and

Cowles. Thus, Claim 11 is allowable over Krause et al. in view of Cowles, Jamal and Grider et al. Claims 12-19, which depend from Claim 11, are allowable over Kraus et al. in view of Cowles, Jamal and Grider et al. for at least the same reasons as Claim 11.

In addition, Claim 18 has been amended to depend from Claim 12 and recite "operating the test modules in response to a first clock signal provided on the test bus during the test mode; and operating the RAM blocks in response to a second clock signal provided on the system circuitry during the test mode, wherein the first clock signal and the second clock signal are independent signals".

The Examiner's rejection seems to indicate that these elements of claim 18 are taught by Jamal.

Jamal teaches that to enter the test mode, "the initialization logic 112 commands the demultiplexer 110 to decouple the RAM from the other components of the integrated circuit die and couples the BIST 100 to the RAM." (Jamal, Col. 6, lines 18-22). Consequently, Jamaal explicitly teaches away from operating the RAM in response to a clock signal provided on the system circuitry during the test mode, as recited by claim 18.

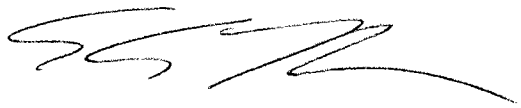
Jamal also teaches that a clock and control signal generator 116 within the BIST 100 generates the internal clock signals used to operate the RAM 84 during the test mode. Jamal further teaches that these internal clock signals are generated in response to the test clock signal received by the BIST 100. (Jamal, column 6, lines 30-40.) Consequently, Jamal teaches away from the use of independent clock signals to operate the test modules and the RAM blocks as recited by claim 18.

For these additional reasons, claim 18 is allowable over Jamaal/Kraus et al./Cowles/Grider et al..

CONCLUSION

Claims 1-19 and 21-22 are pending in the present Application. Reconsideration and allowance of these claims is respectfully requested. If the Examiner has any questions or comments, he is invited to call the undersigned.

Respectfully submitted,



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